

30V N-Channel Enhancement Mode MOSFET

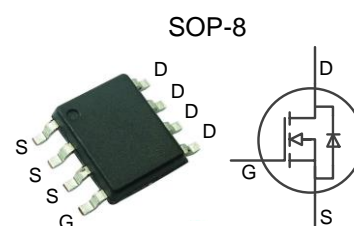
General Features

- Low $R_{DS(ON)}$
- Low Gate Charge
- Advanced high Cell density Trench Technology
- RoHS Compliant
- Halogen-free available
- 100% Avalanche Tested

BV_{DSS}	$R_{DS(ON)}$ @ $V_{GS}=10V$	$R_{DS(ON)}$ @ $V_{GS}=4.5V$
30V	7.3mΩ	9.0 mΩ
I_D	12A	

Applications

- Power Management in Inverter System
- Synchronous Rectification
- Load Switch



Ordering Information

Part Number	Package	Marking	Remark
AKE30N10	SOP-8	30N10	Halogen Free

Absolute Maximum Ratings

 $T_A=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Rating	Unit	
V_{DSS}	Drain-Source Voltage ^[1]	30	V	
V_{GS}	Gate –Source Voltage	±20	V	
I_D	Continuous Drain Current	$T_C=25^{\circ}C$	12	A
		$T_C=100^{\circ}C$	8	A
I_{DP}	300us Pulsed Drain Current Tested ^[2]	48	A	
EAS	Single Pulse Avalanche Energy ^[3]	6.25	mJ	
P_D	Power Dissipation	2	W	
	Derating Factor above 25 °C	0.016	W/ °C	
T_J and T_{STG}	Operating and Storage Temperature Range	-55 ~ 150	°C	

*Drain Current limited by Maximum Junction Temperature.

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	°C /W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	62	°C /W

Electrical Characteristics

OFF Characteristics (TA=25 °C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	30	--	--	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Zero Gate Voltage Drain Current	--	--	1	μA	$V_{DS}=24V, V_{GS}=0V$
I_{GSS}	Gate Leakage Current	--	--	100	nA	$V_{GS}=20V, V_{DS}=0V$
		--	--	-100	nA	$V_{GS}=-20V, V_{DS}=0V$

On Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Drain-Source On-Resistance ^[4]	--	7.3	9.3	m Ω	$V_{GS}=10V, I_D=12A$
		--	9.0	12	m Ω	$V_{GS}=4.5V, I_D=8A$
$V_{GS(TH)}$	Gate Threshold Voltage	1.0	1.4	2.0	V	$V_{DS} = V_{GS}, I_D=250\mu A$
GFS	Forward Transconductance	--	53	--	S	$V_{DS}=5V, I_D=12A$

Dynamic Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	1374	--	pF	$V_{GS}=0V, V_{DS}=15V,$ $f=1MHz$
C_{oss}	Output Capacitance	--	165	--		
C_{rss}	Reverse Transfer Capacitance	--	102	--		
Q_g	Total Gate Charge	--	11	--	nC	$V_{DS}=15V, V_{GS}=4.5V,$ $I_D=8A$
Q_{gs}	Gate-Source Charge	--	2.8	--		
Q_{gd}	Gate-Drain Charge	--	4.8	--		
Rg	Gate Resistance	--	8	--	Ω	f=1MHz

Resistive Switch Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(on)}$	Turn-On Delay Time	--	25	--	ns	$V_{DD}=15V$ $I_D=12A, V_{GS}=10V$ $R_G=3.3\Omega$
t_r	Turn-On Rise Time	--	48	--		
$t_{d(off)}$	Turn-Off Delay Time	--	208	--		
t_f	Turn-Off Fall Time	--	192	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current(Body Diode)	--	--	12	A	Integral P-N diode in MOSFET
I_{SM}	Maximum Pulsed Current(Body Diode)	--	--	48	A	
V_{SD}	Diode Forward Voltage	--	--	1.2	V	$I_{SD}=1A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	--	47	--	ns	$I_{SD}=15A,$ $dI_{SD}/dt=100A/\mu S$
Q_{rr}	Reverse Recovery Charge	--	35	--	nC	

NOTE:

[1] $T_j=+25\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$

[2] Repetitive rating, pulse width limited by maximum junction temperature.

[3] $L=0.5\text{mH}$, $I_{AS}=5A$, Starting $T_j=25\text{ }^{\circ}\text{C}$.

[4] Pulse width $\leq 380\mu\text{s}$; duty cycle $\leq 2\%$.

Typical Characteristics

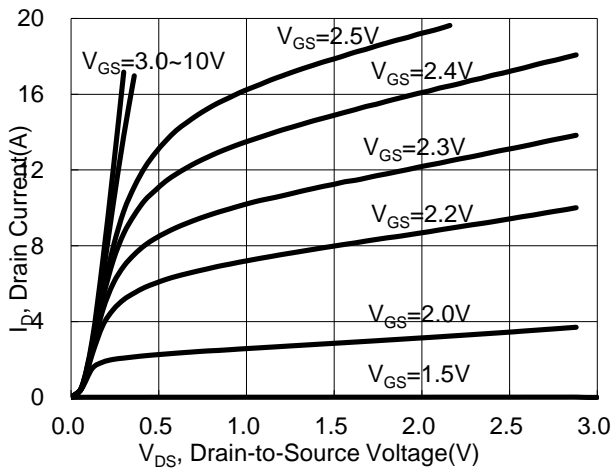
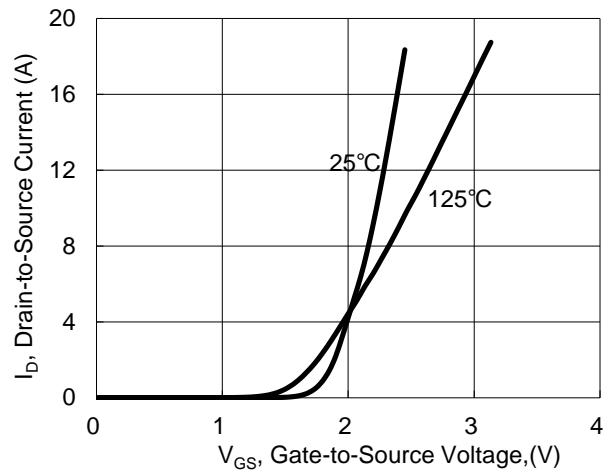
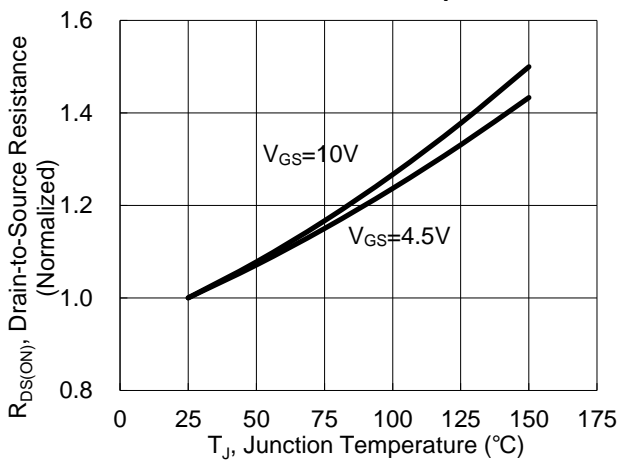
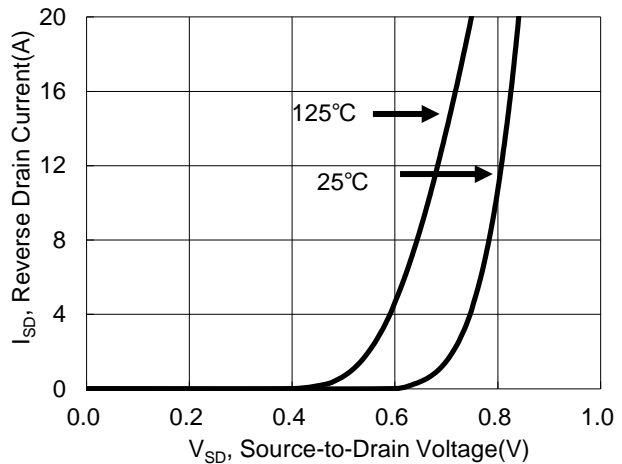
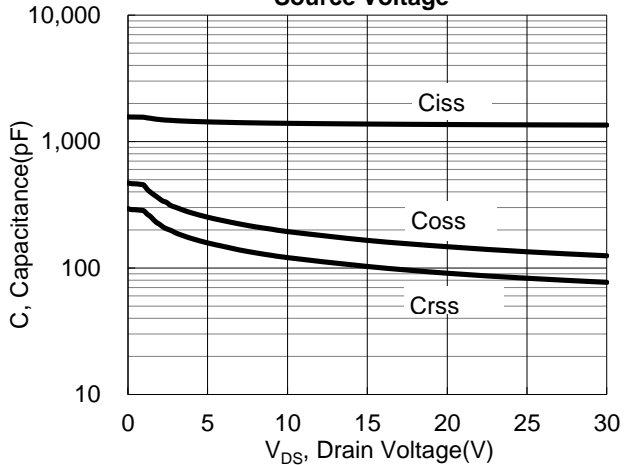
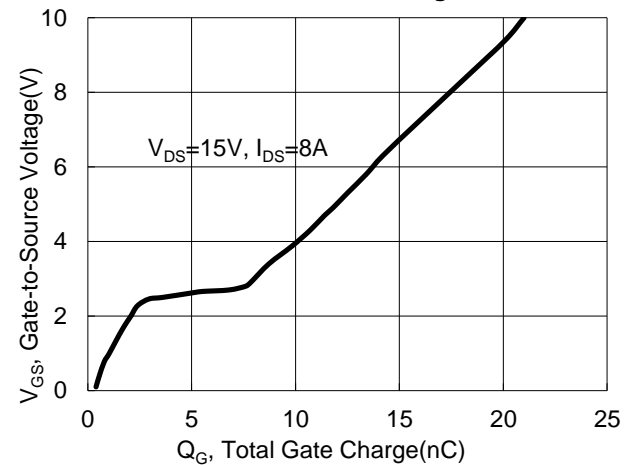
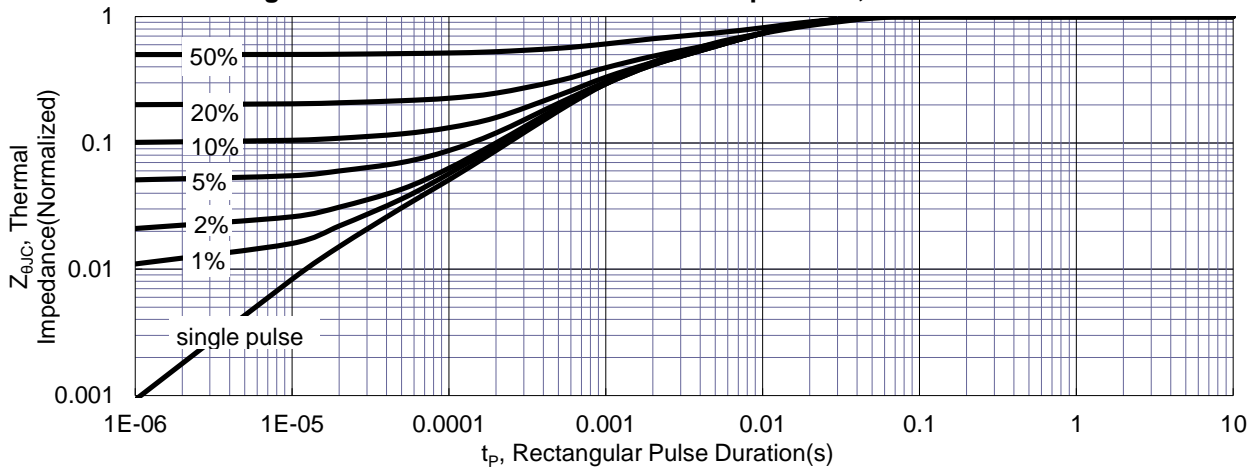
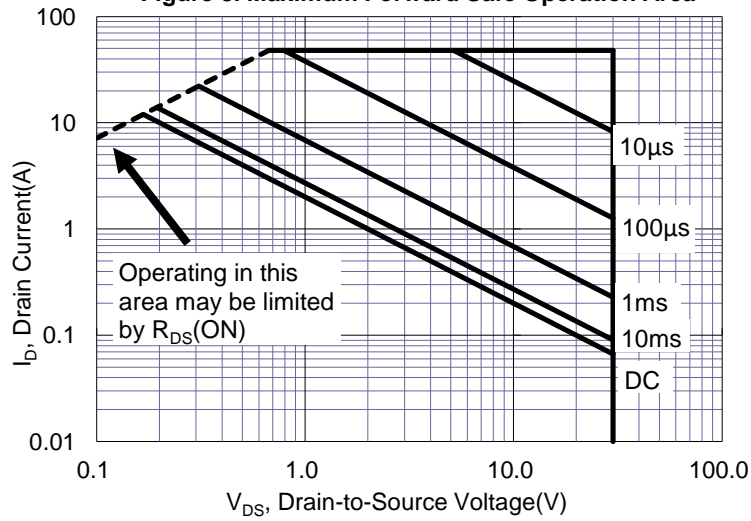
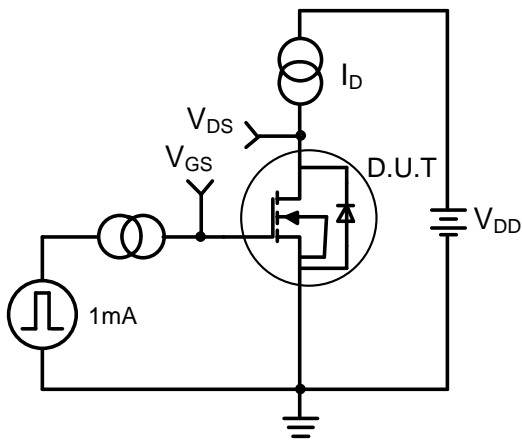
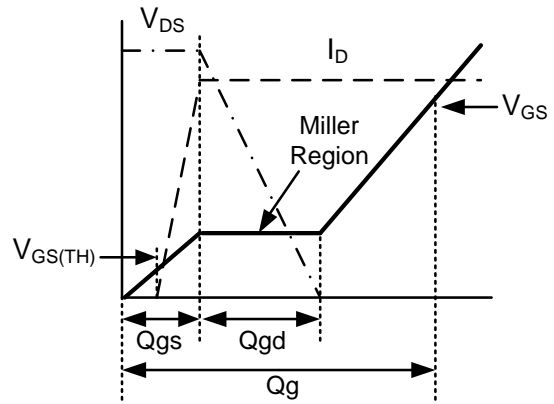
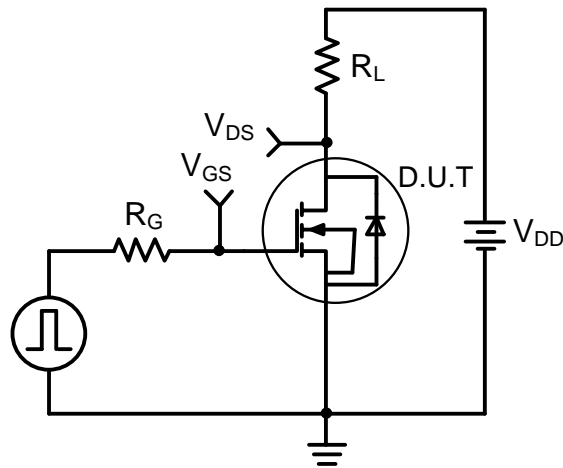
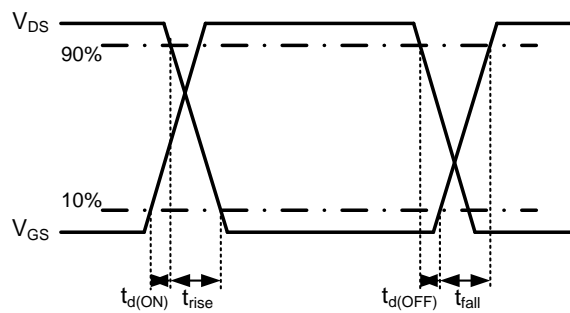
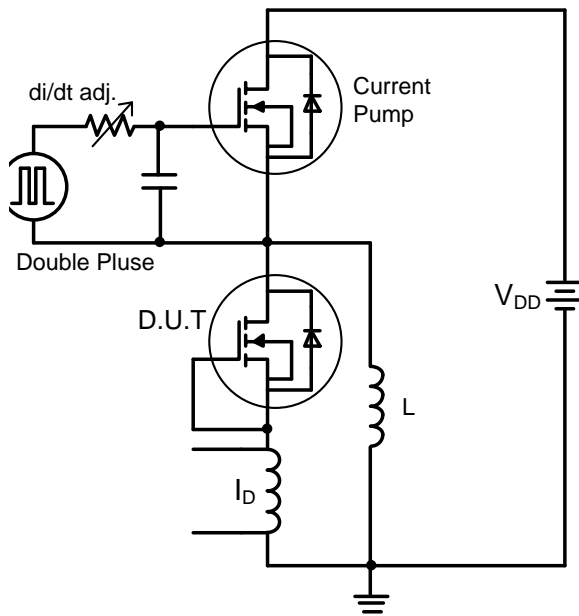
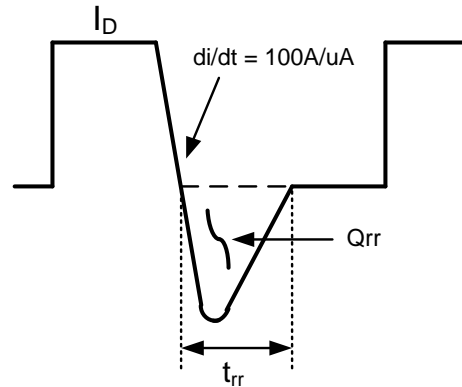
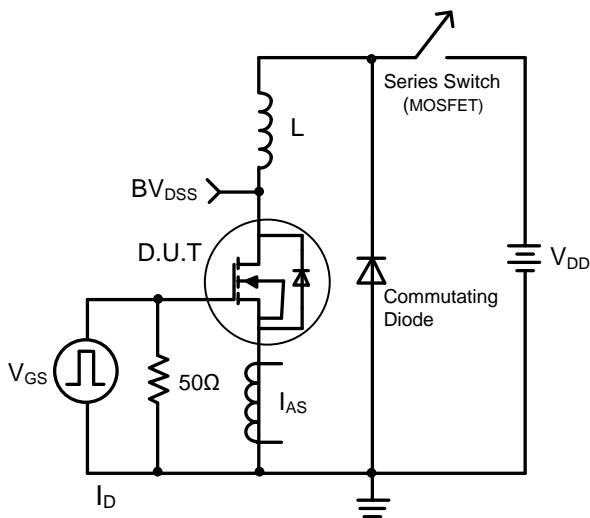
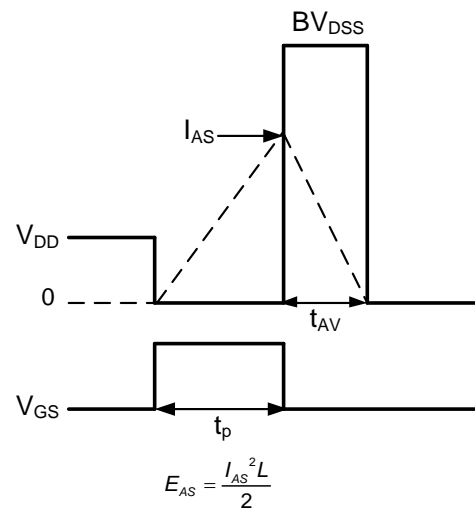
Figure 1. Typical Output Characteristics

Figure 2. Typical Transfer Characteristics

Figure 3. Typical Drain-to-Source On Resistance vs. Junction Temperature

Figure 4. Typical Body Diode Transfer Characteristics

Figure 5. Typical Capacitance vs. Drain-to-Source Voltage

Figure 6. Typical Gate Charge vs. Gate-to-Source Voltage


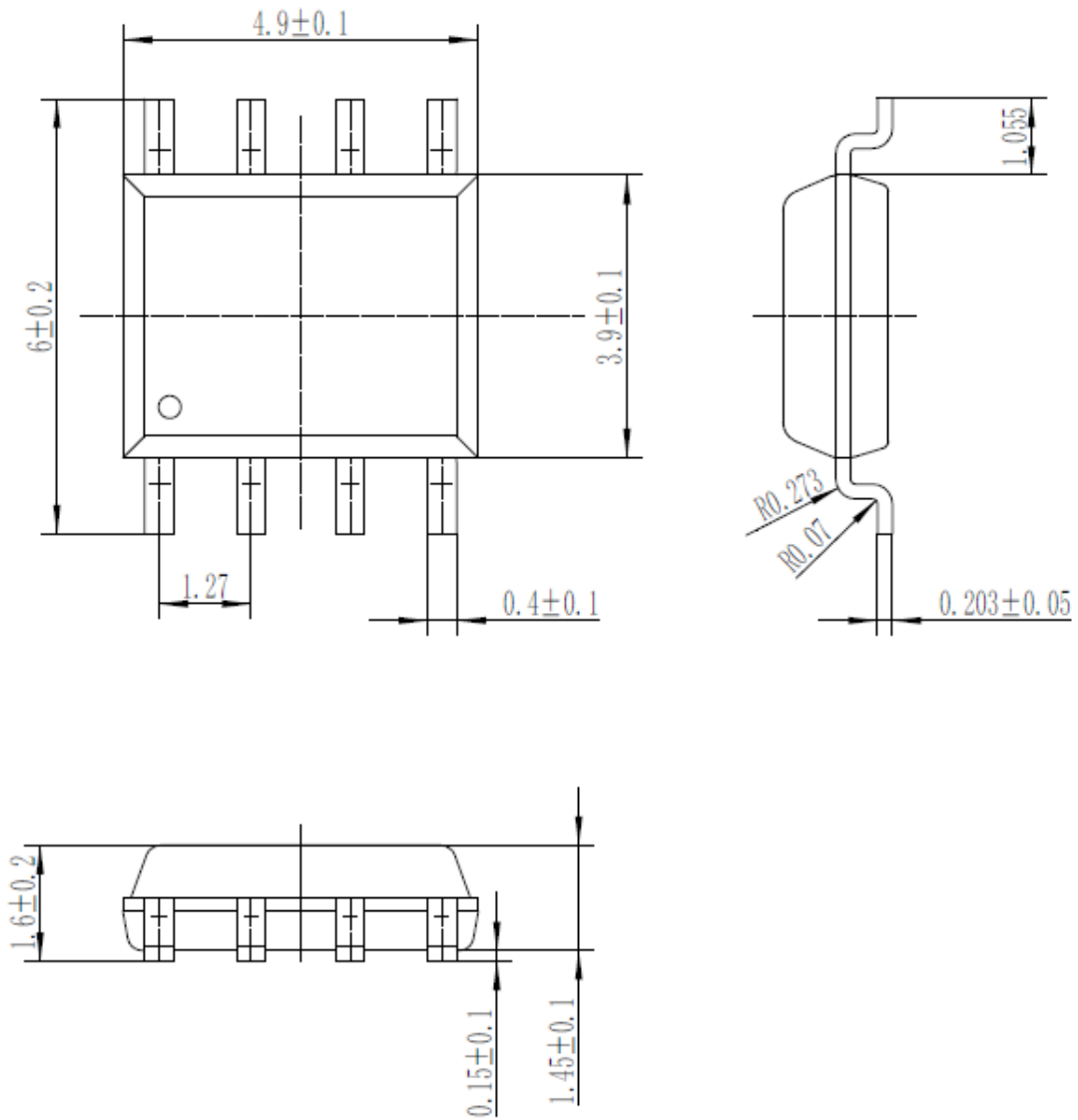
Figure 7. Maximum Effective Thermal Impedance, Junction-to-Case

Figure 8. Maximum Forward Safe Operation Area


Test Circuit

Figure 9. Gate Charge Test Circuit

Figure 10. Gate Charge Waveform

Figure 11. Resistive Switching Test Circuit

Figure 12. Resistive Switching Waveforms


Figure 13. Diode Reverse Recovery Test Circuit

Figure 14. Diode Reverse Recovery Waveform

Figure 15. Unclamped Inductive Switching Test Circuit

Figure 16. Unclamped Inductive Switching Waveforms

Package Dimensions

SOP-8





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ADD: 4F, D26, UESTC National Science Park, No. 1 Shuangxing Avenue, Gongxing Street,
Shuangliu District, Chengdu, China (Sichuan) Pilot Free Trade Zone.
Tel: +86-28-8523-2215 Email: sales@ark-micro.com <http://www.ark-micro.com>

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